CLAIMS

What is claimed is:

1. A method for processing data within a programmable gate array, the method comprises:

detecting, by a fixed logic processor embedded within the programmable gate array, a custom operational code;

providing, by the fixed logic processor, an indication of the custom operational code to the programmable gate array in response to detecting the custom operational code; and

performing, by at least a portion of the programmable gate array configured as a dedicated processor, a fixed logic routine in response to receiving the indication of the custom operational code.

2. The method of claim 1, wherein the detecting the custom operational code further comprises:

executing, by the fixed logic processor, an algorithm that includes a series of instructions from a standard instruction set, wherein the standard instruction set corresponds to an architecture of the fixed logic processor; and

detecting, while executing the algorithm, the custom operational code.

3. The method of claim 1, wherein the providing the indication of the custom operational code further comprises at least one of:

providing data for processing to a portion of the programmable gate array;

providing a co-processing instruction to the at least a portion of the programmable gate array, wherein the co-processing instruction indicates co-processing of the data;

providing a second co-processing instruction to the at

least a portion of the programmable gate array, wherein the second co-processing instruction indicates fetching second data for co-processing;

providing an interrupt instruction to the at least a portion of the programmable gate array, wherein the interrupt instruction indicates interrupt processing of the data;

providing a second interrupt instruction to the at least a portion of the programmable gate array, wherein the second interrupt instruction indicates fetching the second data for interrupt processing; and

providing a system management instruction to the at least a portion of the programmable gate array.

4. The method of claim 1, wherein the providing the custom operational code further comprises:

providing the custom operational code to the at least a portion of the programmable gate array via an auxiliary processing interface of the fixed logic processor.

5. The method of claim 1 further comprises:

generating, by the at least a portion of the programmable gate array, processed data as a result of performing the fixed logic routine; and

providing, by the at least a portion of the programmable gate array, the processed data to the fixed logic processor.

6. The method of claim 5, wherein the providing the processed data further comprises at least one of:

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to providing a data ready indication by the at least a portion of the programmable gate array to the fixed logic processor;

providing, by the at least a portion of the programmable gate array, the processed data to the fixed logic processor upon completion of performing the fixed logic routine; and

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to the fixed logic processor monitoring the performing of the fixed logic routine.

7. The method of claim 1 further comprises:

pre-configuring the at least a portion of the programmable gate array to perform the fixed logic routine.

8. The method of claim 1 further comprises:

detecting, by the fixed logic processor embedded within the programmable gate array, a second custom operational code;

providing, by the fixed logic processor, an indication of the second custom operational code to the programmable gate array in response to detecting the second custom operational code; and

performing, by a second portion of the programmable gate array configured as a second co-processor, a second fixed logic routine in response to receiving the indication of the second custom operational code.

9. The method of claim 1 further comprises:

detecting, by a second fixed logic processor embedded within the programmable gate array, the custom operational code;

providing, by the second fixed logic processor, the indication of the custom operational code to the programmable gate array in response to detecting the custom operational code; and

performing, by at least the portion of the programmable gate array configured as a co-processor, the fixed logic routine in response to receiving the indication of the custom operational code.

10. The method of claim 1 further comprises:

detecting, by a second fixed logic processor embedded within the programmable gate array, a second custom operational code;

providing, by the second fixed logic processor, an indication of the second custom operational code to the programmable gate array in response to detecting the second custom operational code; and

performing, by a second portion of the programmable gate array configured as a second co-processor, a second fixed logic routine in response to receiving the indication of the second custom operational code.

11. A method for processing data within a programmable gate array, the method comprises:

detecting, by a fixed logic processor embedded within the programmable gate array, a custom configuration code;

providing, by the fixed logic processor, an indication of the custom configuration code to the programmable gate array in response to detecting the custom configuration code; and

configuring, by the programmable gate array, at least a portion of programmable gate array as a processor to perform a fixed logic routine in response to receiving the indication of the custom configuration code.

12. The method of claim 11 further comprises:

detecting, by the fixed logic processor, a custom operational code;

providing, by the fixed logic processor, an indication of the custom operational code to the at least a portion of the programmable gate array in response to detecting the custom operational code; and

performing, by the at least a portion of the programmable gate array configured, the fixed logic routine in response to receiving the indication of the custom

operational code.

13. The method of claim 11, wherein the providing the indication of the custom configuration code further comprises at least one of:

providing an indication for a default configuration of the at least a portion of the programmable gate array;

providing an indication that identifies one of a plurality of configurations of the at least a portion of the programmable gate array; and

providing configuration instructions to configure the at least a portion of the programmable gate array.

14. The method of claim 11, wherein the providing the custom configuration code further comprises:

providing the custom configuration code to the at least a portion of the programmable gate array via an auxiliary processing interface of the fixed logic processor.

15. The method of claim 11 further comprises:

detecting, by a fixed logic processor embedded within the programmable gate array, a second custom configuration code;

providing, by the fixed logic processor, an indication of the second custom configuration code to the programmable gate array in response to detecting the custom configuration code; and

configuring, by the programmable gate array, a second portion of programmable gate array as a second processor to perform a second fixed logic routine in response to receiving the indication of the second custom configuration code.

16. The method of claim 11 further comprises:

detecting, by a second fixed logic processor embedded within the programmable gate array, the custom configuration code;

providing, by the second fixed logic processor, the indication of the custom configuration code to the programmable gate array in response to detecting the custom configuration code; and

configuring, by the programmable gate array, the at least a portion of the programmable gate array as the processor to perform the fixed logic routine in response to receiving the indication of the custom configuration code.

17. The method of claim 11 further comprises:

detecting, by a second fixed logic processor embedded within the programmable gate array, a second custom configuration code;

providing, by the second fixed logic processor, an indication of the second custom configuration code to the programmable gate array in response to detecting the second custom configuration code; and

configuring, by the programmable gate array, a second portion of the programmable gate array as a second processor to perform a second fixed logic routine in response to receiving the indication of the second custom configuration code.

18. A field programmable gate array comprises:

logic fabric that includes a plurality of configurable logic blocks, switching blocks, and input/output blocks, wherein at least a portion of the logic fabric is configured as a processor to perform a fixed logic function;

fixed logic processor embedded within the logic fabric; and

auxiliary processing interface that couples the processor to perform the fixed logic function to the fixed logic processor.

19. The field programmable gate array of claim 18 further comprises:

second fixed logic processor embedded with the logic fabric; and

second auxiliary processing interface that couples the second fixed logic processor to the processor to perform the fixed logic function.

20. The field programmable gate array of claim 18 further comprises, wherein a second portion of the logic fabric is configured as a second processor to perform a second fixed logic function:

second auxiliary processing interface that couples the second processor to perform the second fixed logic function to the fixed logic processor.

21. The field programmable gate array of claim 18 further comprises, wherein a second portion of the logic fabric is configured as a second processor to perform a second fixed logic function:

addressing means for enabling the fixed logic processor to address the processor to perform the fixed logic function or the second processor to perform the second fixed logic function.

22. The field programmable gate array of claim 18 further comprises, wherein a second portion of the logic fabric is configured as a second processor to perform a second fixed logic function:

second fixed logic processor embedded with the logic fabric; and

second auxiliary processing interface that couples the second fixed logic processor to the second processor to perform the second fixed logic function.

23. A programmable gate array comprises:

logic fabric that includes a plurality of configurable logic blocks, switching blocks, and input/output blocks;

fixed logic processor embedded within the logic fabric; and

memory operably associated with the fixed logic processor and the logic fabric, wherein, based on operational instructions stored in memory, the fixed logic processor:

detects a custom operational code;

provides an indication of the custom operational code to the logic fabric in response to detecting the custom operational code; and

wherein, based on further operational instructions stored in the memory, at least a portion of the logic fabric:

performs a fixed logic routine in response to receiving the indication of the custom operational code.

24. The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to detect the custom operational code by:

executing an algorithm that includes a series of instructions from a standard instruction set, wherein the standard instruction set correspond to an architecture of the fixed logic processor; and

detecting, while executing the algorithm, the custom operational code.

25. The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to provide the indication of the custom operational code by at least one of:

providing data for processing by the at a portion of the logic fabric;

providing a co-processing instruction to at least a portion of the logic fabric, wherein the co-processing instruction indicates co-processing of the data;

providing a second co-processing instruction to at least a portion of the logic fabric, wherein the second co-

processing instruction indicates fetching second data for co-processing;

providing an interrupt instruction to the at least a portion of the logic fabric, wherein the interrupt instruction indicates interrupt processing of the data;

providing a second interrupt instruction to the at least a portion of the programmable gate array, wherein the second interrupt instruction indicates fetching the second data for interrupt processing; and

providing a system management instruction to the at least a portion of the logic fabric.

26. The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to provide the custom operational code by:

providing the custom operational code to the at least a portion of the logic fabric via an auxiliary processing interface of the fixed logic processor.

27. The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the at least a portion of the logic fabric to:

generate processed data as a result of performing the fixed logic routine; and

provide the processed data to the fixed logic processor.

28. The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the at least a portion of the logic fabric to provide the processed data by at least one of:

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to providing a data ready indication by the at least a portion of the logic fabric to the fixed logic processor;

providing the processed data to the fixed logic processor upon completion of performing the fixed logic routine; and

receiving, from the fixed logic processor, a request for providing the processed data, wherein the request is received in response to the fixed logic processor monitoring the performing of the fixed logic routine.

29. The programmable gate array of claim 23, wherein the memory further comprises operational instructions that cause the fixed logic processor to:

detect a second custom operational code;

provide an indication of the second custom operational code to the logic fabric in response to detecting the second custom operational code; and

wherein, based on further operational instructions stored in the memory, a second portion of the logic fabric performs a second fixed logic routine in response to receiving the indication of the second custom operational code.

30. The programmable gate array of claim 23 further comprises:

a second fixed logic processor, wherein the memory further comprises operational instructions that cause the second fixed logic processor to:

detect the custom operational code;

provide the indication of the custom operational code to the programmable gate array in response to detecting the custom operational code; and

wherein, based on the further operational instructions stored in the memory, the at least a portion of the logic fabric:

performs the fixed logic routine in response to receiving the indication of the custom operational code.

31. The programmable gate array of claim 23 further comprises:

a second fixed logic processor, wherein the memory further comprises operational instructions that cause the second fixed logic processor to:

detect a second custom operational code;

provide an indication of the second custom operational code to the logic fabric in response to detecting the second custom operational code; and

wherein, based on further operational instructions stored in the memory, a second portion of the logic fabric performs a second fixed logic routine in response to receiving the indication of the second custom operational code.

32. A programmable gate array comprises:

logic fabric that includes a plurality of configurable logic blocks, switching blocks, and input/output blocks;

fixed logic processor embedded within the logic fabric; and

memory operably associated with the fixed logic processor and the logic fabric, wherein, based on operational instructions stored in memory, the fixed logic processor:

detects a custom configuration code;

provides an indication of the custom configuration code to the programmable gate array in response to detecting the custom configuration code; and

wherein, based on further operational instructions stored in the memory, the logic fabric configures at least a portion of logic fabric as a processor to perform a fixed logic routine in response to receiving the indication of the custom configuration code.

33. The programmable gate array of claim 32, wherein the memory further comprises operational instructions that cause the fixed logic processor to:

detect a custom operational code;

provide an indication of the custom operational code to the at least a portion of the programmable gate array in response to detecting the custom operational code; and

wherein, based on further operational instructions stored in the memory, the at least a portion of the logic fabric performs the fixed logic routine in response to receiving the indication of the custom operational code.

34. The programmable gate array of claim 32, wherein the memory further comprises operational instructions that cause the fixed logic processor to provide the indication of the custom configuration code by at least one of:

providing an indication for a default configuration of the at least a portion of the logic fabric;

providing an indication that identifies one of a plurality of configurations of the at least a portion of the logic fabric; and

providing configuration instructions to configure the at least a portion of the logic fabric.

35. The programmable gate array of claim 32, wherein the memory further comprises operational instructions that cause the fixed logic processor to provide the custom configuration code by:

providing the custom configuration code to the at least a portion of the logic fabric via an auxiliary processing interface of the fixed logic processor.

36. The programmable gate array of claim 32, wherein the memory further comprises operational instructions that cause the fixed logic processor to:

detect a second custom configuration code;

provide an indication of the second custom configuration code to the programmable gate array in response to detecting the custom configuration code; and

wherein, based on further operational instructions stored in the memory, the logic fabric to configure a second portion of the logic fabric as a second processor to perform a second fixed logic routine in response to receiving the indication of the second custom configuration code.

37. The programmable gate array of claim 32 further comprises:

a second fixed logic processor embedded within the logic fabric, wherein the memory further comprises operational instructions that cause the second fixed logic processor to:

detect the custom configuration code;

provide the indication of the custom configuration code to the logic fabric in response to detecting the custom configuration code; and

wherein, based on the further operational instructions stored in the memory, the logic fabric configures the at least a portion of the logic fabric as the processor to perform the fixed logic routine in response to receiving the indication of the custom configuration code.

38. The programmable gate array of claim 32 further comprises:

a second fixed logic processor embedded within the logic fabric, wherein the memory further comprises operational instructions that cause the second fixed logic processor to:

detect a second custom configuration code;

provide an indication of the second custom configuration code to the logic fabric in response to detecting the second custom configuration code; and

wherein, based on the further operational instructions stored in the memory, the logic fabric configures a second portion of the logic fabric as a second processor to perform a second fixed logic routine in response to receiving the indication of the second custom configuration code, wherein the memory further comprises configuration data that causes

the logic fabric to configure the second processor prior to booting the fixed logic processor or during the booting of the fixed logic processor.